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APPLICATION NO.	FILING DATE	, FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/043,237	01/14/2002	Yasuhiro Doumae	OK1.293 6211		
7590 11/26/2003			EXAMINER		
VOLENTINE FRANCOS, PLLC			. VESPERMAN, WILLIAM C		
Suite 150 12200 Sunrise Vally Drive			ART UNIT	PAPER NUMBER	
Reston, VA 20191			2813		
			DATE MAILED: 11/26/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

					RF				
		Application	on No.	Applicant(s)					
		10/043,23	37	DOUMAE, YASUHIRO					
	Office Action Summary	Examine	•	Art Unit					
		William C	. Vesperman	2813					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply									
A SHOTHE I - Exter after - If the - If NO - Failu - Any r	ORTENED STATUTORY PERIOD FO MAILING DATE OF THIS COMMUNIC sions of time may be available under the provisions of SIX (6) MONTHS from the mailing date of this commu period for reply specified above is less than thirty (30) period for reply is specified above, the maximum statu re to reply within the set or extended period for reply w eply received by the Office later than three months after d patent term adjustment. See 37 CFR 1.704(b).	ATION. 737 CFR 1.136(a). In no evinication. days, a reply within the statutory period will apply and will, by statute, cause the app	ent, however, may a reply be tim utory minimum of thirty (30) day: ill expire SIX (6) MONTHS from lication to become ABANDONE!	nely filed s will be considered time the mailing date of this co O (35 U.S.C. § 133).	ly. ommunication.				
1)⊠	Responsive to communication(s) filed	on <u>08 October 200</u>	<u>13</u> .						
2a)⊠	This action is FINAL . 2b)∐ This action is n	on-final.						
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.								
Disposition of Claims									
5)□ 6)⊠ 7)⊠	Claim(s) 3-6,9-12 and 15-17 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. Claim(s) is/are allowed. Claim(s) 3,5,6,9,11,12,15 and 17 is/are rejected. Claim(s) 4,10 and 16 is/are objected to. Claim(s) are subject to restriction and/or election requirement.								
Application Papers									
9)☐ The specification is objected to by the Examiner. 10)☒ The drawing(s) filed on 14 January 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).									
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.									
Priority under 35 U.S.C. §§ 119 and 120 12)									
2) Notice	ot(s) De of References Cited (PTO-892) De of Draftsperson's Patent Drawing Review (PT De of Disclosure Statement(s) (PTO-1449) Pa		4) Interview Summary 5) Notice of Informal 6 6) Other:						

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DETAILED ACTION

1. This action is in response to applicant's amendment of October 8, 2003.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 3. Claims 3, 5, 6, 9, 11, 12, 15 and 17 are rejected under 35 U.S.C. 102(b) as being anticpated by an article "A Novel Self-aligned Gate-overlapped LDD Poly-Si TFT with High Reliability and Performance", published in the IEEE in 1977 and authored by Mutsuko Hatano, Hajime Akimoto and Takeshi Sakai.

Hatano et al. teaches (Figure 1 and Figure 2) a method of manufacturing a field effect transistor having a semiconductor substrate with a main surface, comprising:

forming a conductive layer of Poly-Si on the main surface with a dielectric film (gate oxide) formed under the conductive layer of Poly-Si, and over the i-poly-Si substrate;

forming a source and drain region in the i-poly-Si surface;

forming pocket regions in the semiconductor i-poly-Si substrate by implanting ions using the mask formed of SiO2 over the conductive layer of Poly-Si;

wherein the SiO2 mask has a width less than a desired width necessary to define a gate length of the gate electrode made of Poly-Si (see Figure 2, step 3 attached), and

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the implanting is carried out from an upward direction of the mask to the semiconductor substrate using the SiO2 mask.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. In regards to Claims 3 and 9, line 3, which state "forming a conductive layer on the main surface <u>via</u> a dielectric film" is indefinite in that the word <u>via</u> is not defined in the applicant's Description of the Preferred Embodiments.

It appears to the examiner that Claims 3 and 9, line 3, should possibly state "forming a conductive layer <u>over</u> a dielectric film formed on the main surface" in order to clarify the claims..

6. Claims 5 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 and 11, lines 2 and 3 respectively state "wherein the gate electrode is formed so as to have a greater width at a top surface than a bottom surface, after the implanting".

Conversely, the Description Of The Preferred Embodiments, page 16, lines 23 - 25, states "the gate electrodes 14a, 14b, and 14c each having a tapered, that is trapezoidal cross-section shape which causes the width of the gate electrodes 14a, 14b and 14c to increase toward a lower direction "and is illustrated in Figures 3(b) and 3(c).

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It appears to the examiner that Claims 5 and 11, lines 2 and 3 respectively should possibly state "wherein the gate electrode is formed so as to have a greater width at a bottom surface than a top surface, after the implanting" in order to be enabled by the Description Of The Preferred Embodiments and Figures 3(b) and 3(c).

Allowable Subject Matter

- 7. Claims 4, 10 and 16 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.
- 8. The following is a statement of reasons for the indication of allowable subject matter.

The prior art does not fairly teach or suggest a method of manufacturing a field effect transistor having a semiconductor substrate with a main surface comprising: forming a conductive layer over a dielectric film formed on the main surface of the substrate; implanting ions to form pocket regions in the semiconductor substrate using a mask formed over the conductive layer; forming a gate electrode by etching the conductive layer using the mask having dielectric spacers formed on side walls of the mask; forming a source region and a drain region in the substrate and in direct contact with the main surface of the substrate, wherein the mask has a width less than a desired width necessary to define a gate length of the gate electrode, and implanting of the ions to form pocket regions in the substrate is carried from an upward direction of the mask to the semiconductor substrate using the mask.

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Conclusion

 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Han et al. (US 5,409,848) teaches an angled pocket implantation semiconductor device.

Tran et al.(US 2002/0068395 A1) teaches a double LDD device.

Wierzorek et al. (US 6,352,885) teaches a transistor having a increased gate insulation.

Dawson (US 6,087,706) teaches a compact transistor structure.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 703-305-1939. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

WCV

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November 17, 2003

ERIK J. KIELIN PRIMARY EXAMINER